

REMARKS

Reconsideration of the application in light of the amendments and the following remarks is respectfully requested.

Status of the Claims

Claims 1 and 4-25 are pending. Claims 2 and 3 have been cancelled without prejudice or disclaimer of the subject matter contained therein. Claims 4-25 have been added. No new matter has been added.

Support for new claims 4-25 can be found, for example, in the Specification on page 3, lines 4-6; page 5, line 22 through page 6, line 23; page 9, line 10 through page 12, line 5; page 13, lines 5-13; page 14, line 16 through page 16, line 5; Table 1; and Figures 1, 5, 7, and 8.

Rejection under 35 U.S.C. §103

Claims 1-3 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Japanese Patent Publication 11-026647 to Junzo in view of U.S. Patent No. 6,961,190 to Tamaoki et al. (“Tamaoki”) and U.S. Patent No. 6,762,496 to Yamamoto et al. (“Yamamoto”). Claims 2 and 3 have been cancelled, thus rendering the rejection moot with respect to claims 2 and 3.

The Examiner contends that Junzo discloses a light-emitting semiconductor element 3 mounted on a substrate 1, where “[i]t is clear from figure 1 that [the distance corresponding to H] . . . is two or three times either length dimension of the semiconductor element, certainly much greater than 0.3 times the length dimension of the semiconductor element.” (Detailed Action, paragraph 3, page 2.) The Examiner further contends that Tamaoki discloses that a typical light emitting area of

an LED is around 1 mm². See, Tamaoki, col. 2, lines 26-30. The Examiner also relies on Yamamoto as disclosing a substrate 1 made from sintered aluminum nitride, which has a thermal conductivity of 190 W/mK, that is 1.5 mm thick. See, Yamamoto, col. 23, line 19; Abstract; and Figure 3. The Examiner contends that it would have been obvious for one of ordinary skill in the art to combine Junzo, Tamaoki, and Yamamoto to achieve the claimed invention.

Applicants note that Junzo fails to provide dimensions for the optical element 3 and the substrate 1, as shown in the computer-generated English language translation of Junzo, attached in **Appendix A**. Thus, Applicants submit that there is no basis for the belief that the Figures provided in Junzo are “to scale” or representative of the actual size of Junzo’s optical element 3 and substrate 1. Therefore, Applicants submit that the Examiner’s contention that “[i]t is clear from figure 1 that this distance [corresponding to H] is two or three times either length dimension of the semiconductor element, certainly much greater than 0.3 times the length dimension of the semiconductor element” (Detailed Action, paragraph 3, page 2) is without merit.

Not notwithstanding the above remarks, Applicants have amended claim 1 to recite “a ratio H/L being greater than or equal to 0.3 but less than 1.25.” As demonstrated in the test results in Table 1, by maintaining the H/L ratio between 0.3 and 1.25, the rate of temperature increase can be controlled to be less than 20%, ensuring that the substrate effectively dissipates the heat generated by the semiconductor element. See, Specification, page 16, line 23 through page 17, line 17 and Table 1.

In contrast, Applicants submit that none of Junzo, Takaomi, or Yamamoto disclose or suggest a H/L ratio that is between 0.3 and 1.25. As noted above, the Examiner contends that Junzo discloses a “distance [that] is two or three times either length dimension of the semiconductor

element, certainly much greater than 0.3 times the length dimension of the semiconductor element (Emphasis Added)." (Detailed Action, paragraph 3, page 2.) Accordingly, Junzo discloses a substrate with a H/L ratio of greater than 2.

Futhermore, the Examiner contends that Yamamoto's substrate is 1.5 mm thick. Thus, the combination of Yamamoto and Tamaoki would result in a substrate with a H/L ratio of 1.5 (*i.e.*, 1.5 mm divided by Tamaoki's 1 mm chip length). Accordingly, both Junzo and the combination of Yamamoto and Tamaoki result in a substrate with a H/L ratio of at least 1.5 or greater. Thus, Junzo, Yamamoto, and Tamaoki, both individually and in combination, fail to disclose or suggest that the ratio H/L is "greater than or equal to 0.3 but less than 1.25," as recited in claim 1.

In addition, MPEP, Section 2144.05(3) states that:

Applicants can rebut a *prima facie* case of obviousness based on overlapping ranges by showing the criticality of the claimed range. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Applicants note that Yamamoto also discloses that the substrate 1 can be 1.2mm thick, which would, in combination with Tamaoki, arguably suggest a H/L ratio of 1.2 (*i.e.*, 1.2 mm/1 mm). See, Yamamoto, col. 19, lines 27-30. However, Applicants submit that the claimed invention has a significant unexpected result of greater heat dissipation in a particular range, which can only be found by varying the H/L ratio through numerous test trials, as in fact were performed by Applicants in this case. As noted above, Applicants have demonstrated in the test results in Table 1 that by maintaining the H/L ratio between 0.3 and 1.25, the rate of temperature increase can be controlled to be less than 20%, ensuring that the substrate effectively dissipates the heat

generated by the semiconductor element. See, Specification, page 16, line 23 through page 17, line 15 and Table 1. In particular, Applicants tests have found that the optimal H/L ratio range is between 0.5 and 1.25, allowing the semiconductor device to have a rate of temperature increase of 5% or less. See, Specification, page 17, lines 15-17. Outside this specific H/L ratio range, the semiconductor device provides substantially inferior heat dissipation performance. For example, at the lower bound of the H/L ratio range, Sample 2 has a H/L ratio of 0.2, resulting in the rate of temperature increase being greater than 20%. Likewise, at the upper bound of the H/L ratio range, Sample 8 has a H/L ratio of 1.5, resulting in the rate of temperature increase jumping to less than 10%; and Sample 9, where the H/L ratio is 2, also results in the rate of temperature increase jumping to less than 10%. See, Specification, page 17, lines 6-15 and Table 1. Thus, as demonstrated by the Applicant, there exists an optimal H/L ratio range which allows for effective heat dissipation of the semiconductor element, which can only be determined through numerous test trials.

Applicants submit that neither Junzo, Yamamoto, or Tamaoki disclose or suggest any motivation or desire to construct a semiconductor device with such a H/L ratio to achieve effective heat dissipation, as demonstrated by the claimed invention. In contrast, Junzo is directed to a surface mounting mold that prevents damage to the plate wiring. See, Junzo, paragraphs 0004-0008. Yamamoto is directed to a process for forming a substrate that has “high thermal conductivity [of the aluminum nitride sintering product], [and] good adhesion properties between the aluminum nitride sintering product and the internal electrically conductive layer” (Yamamoto, col. 1, lines 12-20.) Tamaki is directed to an optical lens formation for use with a light-emitting diode. Thus, none of Junzo, Yamamoto, or Tamaoki are directed at solving the problem addressed

by the claimed invention. Therefore, Applicants submit that the claimed H/L ratio range of 0.3 to 1.25 is nonobvious and patentable over the prior art.

As demonstrated above, the combination of Junzo, Yamamoto, and Tamaoki fail to disclose or suggest each and every element recited in claim 1. Applicants respectfully request reconsideration and withdrawal of the rejection.

Added Claims

Added claims 4-7 depend from claim 1. Applicants submit that added dependent claims 4-7 are patentable for at least the same reasons as discussed above with respect to their base claim.

Added independent claims 8 and 19 recite at least the features of claim 1. Therefore, Applicants submit that added independent claims 8 and 19 are patentable for at least the same reasons as discussed above with respect to claim 1.

Added claims 9-18 depend from claim 8. Added claims 20-22 depend from claim 19. Applicants submit that added dependent claims 9-18 and 20-22 are patentable for at least the same reasons as discussed above with respect to their respective base claim.

Added claims 23-25 are directed to the H/L and H/Y ratios of the semiconductor device. Applicants submit that added claims 23- 25 are patentable over the art of record.

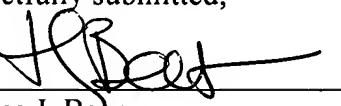
CONCLUSION

Each and every point raised in the Office Action dated April 6, 2006 has been addressed on the basis of the above amendments and remarks. In view of the foregoing it is believed that claims 1 and 4-25 are in condition for allowance and it is respectfully requested that the application be reconsidered and that all pending claims be allowed and the case passed to issue.

If there are any other issues remaining which the Examiner believes could be resolved through a Supplemental Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned at the telephone number indicated below.

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Respectfully submitted,

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